II. AMENDMENTS TO THE CLAIMS:

Please cancel claims 3 and 7 without prejudice. Kindly amend claims 1, 2, 4-6 and 8-20, and add new claim 21, as follows.

The present listing of claims replaces all prior listings, or versions, of claims in the present application.

LISTING OF CLAIMS:

1. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller having a single-chip semiconductor device connecting a Secure Digital Input Output~~SDIO~~-compliant Secure Digital Input Output~~SDIO~~ host device with a plurality of applications via a Secure Digital~~an SD~~ bus, comprising:

(a) a Secure Digital~~an SD~~ interface operably connectable with the Secure Digital Input Output~~SDIO~~ host device to decode commands received from the Secure Digital Input Output~~SDIO~~ host device, and to return a response to the Secure Digital Input Output~~SDIO~~ host device;

(b) ~~one or more~~ application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface; ~~and~~

(c) a temporary memory operably connected between the Secure Digital~~SD~~ interface and ~~the one or more~~ application interfaces; and

(d) a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces.

2. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller according to claim 1, wherein the temporary memory comprises a First-in, First-out~~an R/W FIFO~~ device.

3. (Cancelled)

4. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller according to claim 1, wherein the temporary memory in the ~~SDIO~~Secure Digital Input Output controller comprises as many read memories as the number of application interfaces to temporarily hold data read out of Secure Digital Input Output~~SDIO~~ applications; and at least one write memory operably connected to temporarily hold data to be sent out from~~to~~ the Secure Digital Input Output~~SDIO~~ host.

5. (Currently Amended) A Secure Digital Input Output~~n SDIO~~ controller according to claim 4, wherein each read memory is a First-in, First-out~~RFIFO~~ device and the write memory is a First-in, First-out~~WFIFO~~ device.

6. (Currently Amended) A Secure Digital Input Output~~n SDIO~~ controller according to claim 1, wherein the temporary memory in the Secure Digital Input Output~~SDIO~~ controller comprises at least one read First-in, First-out device~~memory~~ operably connected to temporarily hold data read out of Secure Digital Input Output~~SDIO~~ applications; and at least one write First-in, First-out device~~memory~~ operably connected to temporarily hold data to be sent out from~~to~~ the Secure Digital Input Output~~SDIO~~ host.

7. (Cancelled)

8. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller according to claim 12, further comprising a microcontroller unit for data control, wherein the microcontroller unit is connected to control the Secure Digital~~SD~~ interface and ~~the one or more~~ application interfaces.

9. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller according to claim 8, further comprising an Input/Output~~I/O~~ device connected to input and output control signals to and from the microcontroller unit.

10. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller according to claim 9, wherein the Input/Output~~I/O~~ device is a general peripheral Input/Output~~I/O~~ device.

11. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ controller according to claim 10, wherein the microcontroller unit operates to decode data when the data sent from the Secure Digital Input Output~~SDIO~~ host device to the Secure Digital Input Output~~SDIO~~ controller via the Secure Digital~~SD~~ bus contains at least a register read/write address, a selected type of operation, a quantity of data, and arbitrary write data in a digital system, and the microcontroller unit operates to access non-contiguous registers via an application interface.

12. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications card comprising:

(a) a Secure Digital Input Output~~an SDIO~~ controller comprising:

(i) a Secure Digital~~an SD~~ interface operably connectable with the Secure Digital Input Output~~SDIO~~ host device to decode commands received from the Secure Digital Input Output~~SDIO~~ host device, and to return a response to the Secure Digital Input Output~~SDIO~~ host device;

(ii) ~~one or more~~ application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface; ~~and~~

(iii) a temporary memory operably connected between the Secure Digital~~SD~~ interface and ~~the~~ one or more application interfaces;

(b) a wireless communications module operably connected to the Secure Digital Input Output~~SDIO~~ controller via the one or more application interfaces; ~~and~~

(c) a Secure Digital Input Output~~an SDIO~~-compliant card enclosure, wherein the Secure

Digital Input Output~~SDIO~~ controller and the wireless communications module are disposed within the enclosure; and

(d) a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces.

13. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications card according to claim 12, wherein the temporary memory comprises ~~an~~ a Read/Write First-in, First-out~~R/W FIFO~~ device.

14. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications card according to claim 13, wherein the Secure Digital Input Output~~SDIO~~ controller further comprises a microcontroller unit for data control, wherein the microcontroller unit is operably connected to control the Secure Digital~~SD~~ interface and ~~the~~ one or more application interfaces.

15. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications card according to claim 14, wherein the wireless communications module is selected from the group consisting of a IEEE 802.11b module, a IEEE 802.11a module, a IEEE 802.11e module, and a IEEE 802.11g module~~, and a Bluetooth module~~.

16. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications card according to claim 14~~15~~, further comprising one or more additional applications selected from the group consisting of a global positioning system and a personal handyphone system, wherein the one or more additional applications are operably connected to corresponding application interfaces of the Secure Digital Input Output~~SDIO~~ controller.

17. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications module comprising:

(a) a Secure Digital Input Output~~an SDIO~~ controller comprising:

(i) a Secure Digital~~an SD~~ interface operably connectable with the Secure Digital Input Output~~SDIO~~ host device to decode commands received from the Secure Digital Input Output ~~SDIO~~ host device, and to return a response to the Secure Digital Input Output~~SDIO~~ host device;

(ii) ~~one or more~~ application interfaces selected from the group consisting of a PCMCIA interface, a PC card bus interface, and a UART interface; ~~and~~

(iii) a temporary memory operably connected between the Secure Digital~~SD~~ interface and ~~the one or more~~ application interfaces; and

(iv) a First-in, First-out controller comprising a direct memory access controller operably connected to transfer data between the temporary memory and the application interfaces; and

(b) a wireless communications module operably connected to the Secure Digital Input Output~~SDIO~~ controller via the one application interface; wherein the Secure Digital Input Output~~SDIO~~ controller and the wireless communications module are integrated on a single circuit chip to form the Secure Digital Input Output~~SDIO~~ wireless communications module.

18. (Currently Amended) A Secure Digital Input Output~~An SDIO~~ wireless communications module according to claim 17, wherein the temporary memory comprises a Read/Write First-in, First-out~~an R/W FIFO~~ device.

19. A~~n~~ wireless communications module~~eard~~ according to claim 18, wherein the Secure Digital Input Output~~SDIO~~ controller further comprises a microcontroller unit for data control, wherein the microcontroller unit is operably connected to control the Secure Digital~~SD~~ interface and the one or more application interfaces.

20. (Currently Amended) A method of transmitting write data from a Secure Digital Input Output~~an SDIO~~ host device to a Secure Digital Input Output~~an SDIO~~ application, the method comprising the steps of:

(a) connecting a Secure Digital Input Output~~an SDIO~~ application with a Secure Digital Input Output~~an SDIO~~ host device, wherein the Secure Digital Input Output~~SDIO~~ application comprises a Secure Digital Input Output~~an SDIO~~ controller having a Secure Digital~~an SD~~ interface and an application interface;

(b) receiving a write command from the Secure Digital Input Output~~SDIO~~ host device via the Secure Digital~~SD~~ interface and interpreting the command;

(c) generating a command response signal using the Secure Digital~~SD~~ interface and sending the command response signal to the Secure Digital Input Output~~SDIO~~ host device;

(d) after the Secure Digital Input Output~~SDIO~~ host device receives the command response signal, transmitting data from the host device to the Secure Digital Input Output~~SDIO~~ controller via the Secure Digital~~SD~~ interface, wherein the transmitted data includes at least a register read/write address, a selected type of operation, a quantity of data, and arbitrary write data in a digital system;

(e) decoding the transmitted data using a microcontroller unit of the Secure Digital Input Output~~SDIO~~ controller; and

(f) accessing non-contiguous register addresses of registers~~SD memory~~ in the Secure Digital Input Output~~SDIO~~ application via the application interface by using the microcontroller unit so data sent from the Secure Digital Input Output~~SDIO~~ host device is written into the registers~~SD memory~~ of the Secure Digital Input Output~~SDIO~~ application.

21. (NEW) A Secure Digital Input Output controller according to claim 1, wherein the temporary memory comprises one First-in, First-out device for writing data and three First-in, First-out devices for reading data.